module sync\_basic\_block\_1(reset\_n, clk\_in, data\_in, data\_out);

parameter a\_length = 3;

input [a\_length-1:0] data\_in;

output reg [a\_length-1:0] data\_out;

reg [a\_length-1:0] dff\_1;

input clk\_in, reset\_n;

always@(posedge clk\_in or negedge reset\_n)

begin

if(~reset\_n)

dff\_1<=3'b0;

else

dff\_1<=data\_in;

end

always@(posedge clk\_in or negedge reset\_n)

begin

if(~reset\_n)

data\_out<=3'b0;

else

data\_out<=dff\_1;

end

endmodule